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(54) Title of the Invention: FORMATION OF ACTIVE MATRIX LIQUID CRYSTAL DISPLAY AND DRIVING METHOD THEREFOR

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Specification

1. Title of the Invention

FORMATION OF ACTIVE MATRIX LIQUID CRYSTAL DISPLAY AND DRIVING METHOD THEREFOR

2. Scope of Claim

(1) In a method of forming an active matrix liquid crystal display, a method of forming the active matrix liquid crystal display characterized by producing the liquid crystal display by combining a photolithographic step and a resist printing step.

(2) In a method of forming an active matrix liquid crystal display, a method of forming the active matrix liquid crystal display characterized by forming a built-in peripheral circuit in a photolithographic step and a display part in a resist printing step.

(3) In a method of forming an active matrix liquid crystal display, a method of forming the active matrix liquid crystal display characterized by using a photolithographic step only in forming a channel length L of a TFT of a display part and doing the other processes in resist printing steps.

(4) In a method of forming an active matrix liquid crystal display, a method of forming the active matrix liquid crystal display characterized by positioning a built-in peripheral circuit formed in a photolithographic step in as narrow region as possible.

(5) In a driving method of an active matrix liquid crystal display, a driving method of the active matrix liquid crystal display characterized by:

producing a plurality of peripheral driving circuits formed in photolithographic steps on a glass substrate; and

driving a display part with one or those of the built-in peripheral circuits that have no defects.

(6) In a driving method of an active matrix liquid crystal display, a driving method of the active matrix liquid crystal display characterized by:

dividing a built-in peripheral circuit formed in a photolithographic step into plural; and

substituting a COG (Chip ON GLASS) for one or those of the built-in peripheral circuits which have some defects.

(7) In a driving method of an active matrix liquid crystal display, a

driving method of the active matrix liquid crystal display characteriz d by substituting an external peripheral circuit for a defective part of th built-in peripheral circuits formed in a photolithographic step.

3. Detailed Description of the Invention

[Industrial Field for the Invention]

The present invention relates to an active matrix liquid crystal display, particularly a formation of a large area liquid crystal display and a driving method therefor.

[Prior Art]

Conventionally, a constitution of an active matrix liquid crystal display is described, for example, in 1988 INTERNATIONAL DISPLAY RESEARCH CONFERENCE DIGEST pp.215 to 219. Here the above structure is shown in Fig. 2. In Fig. 2, reference number 1 denotes a glass substrate, 2 denotes a display part, 6 denotes a driving circuit on a scanning side, and 7 denotes a driving circuit on a signal side. All the above structures are formed in photolithographic steps.

[Problems to be Solved by the Invention]

When a large area display of the above conventional structures is produced by photolithographic steps, low throughput is obtained since a throughput capacity of the photolithographic step itself is slow and it is impossible to process a large amount of large area substrates at a time. On the other hand, when a large area display of the above conventional structures is produced by resist printing steps, higher throughput can be obtained, but it is difficult to form a built-in peripheral circuit which needs to be comparatively finely processed. The purpose of this invention is to produce the large area display of the above conventional structures with high throughput.

[Means for solving the Problems]

The purpose above is achieved by producing a liquid crystal display by combining a photolithographic step and a resist printing step.

[Operation]

In the process above, since a resist printing step is used as a part of process, throughput is improved. Also, the photolithographic step is used for constituting a built-in peripheral circuit and the like, which needs to be comparatively fin ly processed, so that a normal built-in peripheral circuit can be formed. Thus, by the present invention, an active matrix liquid

crystal display with a built-in peripheral circuit can be produced with high throughput.

[Embodiment]

An embodiment of the present invention follows with reference to Fig. 1.

Fig. 1 shows an embodiment of the present invention. In Fig. 1, reference number 1 denotes a glass substrate, 5 denotes a display part formed in a resist printing step, 6 denotes a driving circuit on a scanning side which is a part of the peripheral circuits formed in photolithographic steps, and 7 denotes a driving circuit on a signal side which is a part of peripheral circuits formed in photolithographic steps. Namely, by using both the photolithographic step and the resist printing step as a constituting process of Fig. 1, throughput is improved.

Fig. 3 is an embodiment of a pattern of a display part in the case where the present invention is used. In Fig. 3, reference number 10 denotes a signal electrode, 11 denotes a scanning electrode, 12 denotes a contact hole, 13 denotes an extrinsic polycrystalline silicon film, 14 denotes an ITO, reference symbol W denotes a channel width, and L denotes a channel length. Here, as a means of improving the current driving performance of TFTs, there is a way to shorten the channel length L. For the above reason, in Fig. 3, the photolithographic step is used only for a process of forming the channel length L, namely, for forming the scanning electrode 11, and the resist printing step is used for the other processes. By using the process above, high throughput of a liquid crystal display and high performance of TFTs are accomplished.

Fig. 4 is an embodiment in the case where the present invention is applied to a liquid crystal display with a built-in peripheral circuit. In Fig. 4, reference number 1 denotes a glass substrate, 5 denotes a display part formed in the resist printing step, 6 denotes a driving circuit on a scanning side which is a part of the peripheral circuits formed in the photolithographic steps, and 7 denotes a driving circuit on a signal side which is a part of peripheral circuits formed in the photolithographic steps. In Fig. 4, the peripheral circuits are formed in as narrow region as possible. In an LSI, yield is proportionate to area. For the reason above, the yield of the peripheral circuits in Fig. 4 improves, and so does the throughput of the liquid crystal display.

Fig. 5 is an embodiment in the case where the present invention is appli d to a crystal display with a built-in peripheral circuit. In Fig. 5, reference number 1 denotes a glass substrate, 5 denotes a display part formed in the resist printing step, 6-1 to 6-N each denotes a driving circuit on a scanning side which is a part of the peripheral circuits formed in the photolithographic steps, and 7-1 to 7-M each denotes a driving circuit on a signal side which is a part of the peripheral circuits formed in the photolithographic steps. In Fig. 5, one or those of the driving circuits on a scanning side which have no defects, 6-1 to 6-N, and one or those of the driving circuits on the signal side which have no defects, 7-1 to 7-M, drive the display part 5. For this reason, the yield of the peripheral circuits in Fig. 5 improves, and so does the throughput of the liquid crystal display.

Fig. 6 is an embodiment in the case where the present invention is applied to a liquid crystal display with a built-in peripheral circuit. In Fig. 6, reference number 1 denotes a glass substrate, 5 denotes a display part formed in the resist printing step, 6-1 to 6-N each denotes a driving circuit on a scanning side which is a part of peripheral circuits formed in the photolithographic steps, and 7-1 to 7-M each denotes a driving circuit on a signal side which is a part of the peripheral circuit formed in the photolithographic steps. In Fig. 6, one or those of the driving circuits on a scanning side which have no defects, 6-1 to 6-N, and one or those of the driving circuits on a signal side which have no defects, 7-1 to 7-M, drive the display part 5. For this reason, the yield of the peripheral circuits in Fig. 6 improves, and so does the throughput of the liquid crystal display.

Fig. 7 is an embodiment in the case where the present invention is applied to a liquid crystal display with a built-in peripheral circuit. In Fig. 7, reference number 1 denotes a glass substrate, 5 denotes a display part formed in the resist printing step, 8-1 to 8-N are parts of a driving circuit on a scanning side which is formed in the photolithographic step and divided into N, and 9-1 to 9-M are parts of a driving circuit on a signal side which is formed in the photolithographic step and divided into M. In the structure shown in Fig. 7, for example, even if there are some defects in section 9-2 and 8-N as shown in Fig. 7 (a), a COG (Chip on GLASS) can be substitute for the defective parts as shown in Fig. 7 (b). From the above, the throughput of the liquid crystal display improves by the above deficiency solution.

Fig. 8 is an embodiment in the case where the present invention is applied to a liquid crystal display with a built-in peripheral circuit. In Fig. 8, reference number 1 denotes a glass substrate, 5 denotes a display part formed in the resist printing step, 7 denotes a driving circuit on a signal side formed in the photolithographic step, and 6 denotes a driving circuit on a scanning side formed in the photolithographic step. In the structure shown in Fig. 8, for example, even if there are some defects in the driving circuit on the scanning side 6 as shown in Fig. 8 (a), an external driving circuit on the scanning side (IC: INTEGRATED CIRCUITS) can be a substitute for the defective part as shown in Fig. 8 (b). From the above, the throughput of the liquid crystal display improves by the above deficiency solution.

[Effect of the invention]

According to the present invention, a large area liquid crystal display with a built-in peripheral circuit can be produced with high throughput. Thus, there are the advantages of accomplishing high performance and cost reduction and so on of the liquid crystal display.

4. Brief Description of the Drawings

Fig. 1, Fig. 4, Fig. 5, Fig. 6, Fig. 7 and Fig. 8 show plan views showing structures of liquid crystal displays with built-in peripheral circuits which are embodiments of the present invention, Fig. 2 shows a plan view showing a structure of a conventional liquid crystal display with a built-in peripheral circuit, and Fig. 3 shows a plan view showing a structure of a display part of a liquid crystal display which is an embodiment of the present invention.

1···A glass substrate

2···A display part formed in a photolithographic step

5···A display part formed in a resist printing step

6···A driving circuit on a scanning side formed in a photolithographic step

6-1 to 6-N···A plurality of driving circuits on a scanning side formed in a photolithographic step

7···A driving circuit on a signal side formed in a photolithographic step

7-1 to 7-M···A plurality of driving circuits on a signal side formed in a photolithographic step

8-1 to 8-N···Parts of a driving circuit on a scanning side which is formed in

a photolithographic step and divided into N

9-1 to 9-M···Parts of a driving circuit on a signal side which is formed in a photolithographic step and divided into M

COG···Chip on GLASS

10···A signal electrode

11···A scanning electrode

12···A contact hole

13···An extrinsic polycrystalline silicon film

14···ITO

W···A channel width

L···A channel length

Fig. 1

1···A glass substrate

5···A display part formed in a resist printing step

6···A driving circuit on a scanning side formed in a photolithographic step

7···A driving circuit on a signal side formed in a photolithographic step

DRIVE LSI PACKAGING TECHNOLOGY

PROBLEM SOLVING BY COG AIMING FOR HIGH DEFINITION

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The packaging technology of drive LSI has been popularly applying TAB (tape automated bonding). However, if the terminal pitch is narrowed down to 100 μm, an obstacle arises. To overcome the obstacle, essentially required is the COG (chip on glass) technology. Some methods are now in practical use out of various others so far proposed. For the purpose of realizing high-definition panels, research is under way to challenge reliability, checkup, facility, and the like.

Making full use of characteristics such as lightweightness, slimness, driving-power thriftiness, better alignment with LSI, and the like, liquid crystal displays have become popular. In recent years, with improved liquid crystal materials and developed fine-pixel processing technology, for example, image quality has been acceleratingly enhanced, and the application range has been significantly widened. The extensive applications have been studied, aiming for new fields and hoping CRT replacement. Exemplarily considered are applications to small-sized high-definition displays such as clocks, calculators, measuring instruments, view finders, and

projection displays (projectors), and large-sized multiple-pixel displays such as personal computers, work stations, and television sets.

PROBLEM OF CONNECTION, MANY IN NUMBER AND HIGH DENSITY

FIG. 1 shows the relationship between screen size and pixel electrode pitch on an application basis of liquid crystal panels. Due to upsizing of the liquid crystal panels with higher-definition, technology development has been a big concern, i.e., surely technology of high-density multi-terminal liquid crystal panel formation, and technology of high-terminal-density connection between a pixel electrode and a drive LSI.

As the drive LSI packaging technology of liquid crystal panels, currently applied has been such a packaging technology as shown in FIG. 2.

FIG. 2(a) shows the packaging structure so far popularly applied to monochrome liquid crystal panels for OA equipment with pixel electrode pitch of 300 μm or more. In the structure, a print wiring board is packaged with a QFP (quad flat package) of about 80 outputs or a pair-chip drive LSI, and connected with the pixel electrodes of the liquid crystal panel via an anisotropic-conductive rubber connector or a heat seal connector. FIG. 2(b) shows the TAB (tape automated bonding) packaging structure so far most popularly applied to

high-pixel-density liquid crystal panels such as liquid crystal televisions, and color liquid crystal panels mainly for OA. In the structure, a drive LSI chip is packaged into a tape carrier, and connected with pixel electrodes of the liquid crystal panel via an ACF (anisotropic conductive film).

FIG. 2(c) shows the COG (chip on glass) packaging structure having been in practical use for a part of high-pixel-density liquid crystal panels. In the structure, a drive LSI chip is directly packaged onto the glass substrate of the liquid crystal panel.

Other than those structures, as an exemplary structure having been in practical use for very limited products, a polycrystalline Si TFT liquid crystal panel having a driving circuit formed simultaneously with a transistor formed to a pixel section.

QUITE A FEW CAPABILITY REQUIREMENTS SUCH AS COST

As to drive LSI packaging of liquid crystal panels, there needs to satisfy the following requirements as much as possible.

1. Capable of forming liquid crystal panel modules compact in size - leading to downsizing in terms of capacity and area.

2. Capable of responding to fine-pitch, multi-terminal electrode connection - requiring connection using about 2000 electrodes with electrode pitch of 100 μm or lower, in consideration of the relationship between the number of

electrode and pitch of a side of the pixel electrode derived from the pixels of the liquid crystal panel.

3. Resistance value relating to connection of drive LSI including pixel electrode pattern resistance being low, and uniform between pixel electrodes.

4. Low-price packaging is possible - meeting expectations of the fewer packaging processes, the fewer components for use, and higher packaging yield.

5. Easy checkup of liquid crystal panel, drive LSI, and liquid crystal panel module.

6. Satisfying reliability level consistence with application of liquid crystal panel.

7. Allowing exchange of drive LSI - repairing is important due to plural connection of multi-terminal drive LSI to high-value-added liquid crystal panel.

COG - REDUCED IN PRICE AND HIGH-DENSITY CAPABLE

With respect to high-definition liquid crystal panels to be expanded from now on, COG is considered promising as the packaging structure of drive LSI satisfying the above requirements, and thus various manufacturers are now considering its feasibility.

The reason why promising includes the following two factors:

1. Having good chance of drive LSI packaging lower in

price and better in quality stability - exemplarily compared with TAB packaging, achieving the fewer components for use, the fewer packaging processes, the less packaging equipment, and smaller area of the drive LSI chip.

2. Advantageous for connection of high-density multi-terminal - compared with TAB packaging, allowing detailed pattern processing for drive LSI packaging. Having less connection constraints (cumulative pitch error of substrate pattern / ACF resolving power / positioning error between substrate and liquid crystal panel) regarded as a problem for TAB packaging.

However, due to the reasons such as better production equipment, higher actual usage, higher reliability in terms of quality, and the like, the TAB packaging will be widely applied, for the time being, to liquid crystal panels of connection pitch being 100 μm or more.

Here, the technology of forming drive circuits to polycrystalline Si TFT liquid crystal panels is considered promising in the future in terms of applications to various fields. As to progress relating to the liquid crystal panels, however, the technology may be limitedly applied to those smaller in size and higher in density considering yield, and the like.

TAB PACKAGING WILL BE APPLIED TO LCD OF 100μm OR MORE FOR THE TIME BEING

The TAB packaging has currently been mainstream of drive LSI packaging for high-definition liquid crystal panels. This is because of fine-pitch of tape carriers, improved technology of multi-terminal pattern processing, improved ACF connection resolving power (pitch and area), developed TAB packaging associated equipment by equipment manufacturers, and the like.

FIG. 4 is a diagram showing the process concept of drive LSI packaging by TAB packaging.

Electrode sections of a drive LSI are each formed with an Au bump having a height of 20 μm or more. Other than that, on an exemplary polyimide film, a Cu pattern is formed, and an Au or Sn coating is applied thereto so as to derive a carrier tape. Then, a bump of the drive LSI is connected thereto by one operation by thermocompression bonding.

Then, the drive LSI section is sealed by resin, and after a checkup, only conforming items are separated from the carrier tape (outer lead observed). This and the electrodes on the liquid crystal panel are connected together via an ACF. In such a manner, the TAB packaging is generally done.

400 OUTPUTS ACHIEVED IN PROTOTYPING ASSESSMENT STAGE

Shown below is the present level of TAB packaging having been applied to the current drive LSI packaging.

- The number of output terminals : 120 outputs, mainly 160 outputs (140 to 200 terminals in total).

- ILB (inner lead bonding) pitch : most popularly 100 to 120 μm pitch (reported case of lowest pitch being 80 μm).
- OLB (outer lead bonding) pitch : vary depending on liquid crystal panel (reported case of lowest pitch being 100 to 120 μm).

In order to respond to high-definition liquid crystal panels of the future, a fine-pitch multi-terminal TAB packaging technology has been under development. At this point in time, prototypes with 240 to 400 outputs manufactured by the TAB packaging have been subjected to assessment.

PROBLEM OF PRICE, CONNECTION RESOLVING POWER, AND CHECKUP

Such TAB packaging has the following advantages:

1. Time-proven actual usage, and higher reliability in terms of quality, for example.

2. Allowing any existing TAB packaging equipment (for example, bonding unit, sealing unit, handler, thermocompression bonding unit for ACF) to be used.

3. Allowing a drive LSI determined as a conforming item after a checkup to use for connection with a liquid crystal panel.

4. Reducing area for connection between a liquid crystal panel and a drive LSI.

On the other hand,

1. Difficulty in packaging price reduction due to many

required components such as an expensive polyimide tape carrier, a print wiring substrate, and the like, and many packaging processes.

2. Requiring equipment adaptable for connection due to many connection points such as ILB (connection between a drive LSI and a tape carrier), OLB (connection between a TAB packaging substrate and a liquid crystal panel).

3. Difficulty in multi-terminal OLB with fine-pitch lower than 100 μm due to limitations of tape carrier pattern processing, constraints of connection resolving power between a TAB substrate electrode and a liquid crystal panel.

4. The more electrodes for TAB packaging, the more obvious the reduction in contact stability at the time of checkup, and the increase in electrode area for checkup become. As such, there are still many challenges left including packaging price, fine-pitch multi-terminal pattern processing technology, OLB technology, and checkup technology.

ACHIEVING 40 μm USING THIN Cu FOIL HIGH IN TENSILE STRENGTH

In a case of using a current 1-ounce Cu foil, the TAB pattern processing level has a processing limitation of 80 μm pitch. Further, with respect to the fine-pitch pattern processing, the easiest way to cope with is to thinning the Cu foil. However, thinning the Cu foil resultantly reduces the strength of lead electrodes.

Thus, there needs to reduce the electrode pitch without reducing the strength of lead electrodes using the Cu foil high in tensile strength. Presently, it now may not be impossible to perform TAB tape carrier processing of lead electrode pitch being 40 μm using a 1/2 ounce Cu foil high in tensile strength.

Connection between a TAB packaging substrate and an electrode of a liquid crystal panel is susceptible to cumulative pitch error, connection resolving power of ACF, positioning error between TAB pattern and electrode of liquid crystal panel, and the like, all caused by TAB pattern processing and surrounding environment.

NEED FOR CONNECTION TECHNOLOGY IN PLACE OF ACF

Therefore, with connection using an ACF (anisotropic conductive film), about 200 terminals with electrode pitch of 100 μm are presently a connectable level at one time. FIG. 3 shows the result of a trial calculation about the relationship between the connection pitch and the number of terminals connectable for one time connection, with a TAB tape accuracy of 0.05%, an ACF resolving power of 80 μm, and a positioning accuracy of ±10 μm.

To deal with connection with the finer pitch and the more terminals, as a new connection method in place of ACF connection, so far developed is the following connection methods.

The UV adhesive method developed by Matsushita Electric

Industrial, Co., Ltd. is a method for directly connecting the pixel pattern of a liquid crystal panel and a TAB electrode using an UV adhesive. This method allows connection without suffering from constraints of ACF resolving power, suiting for high-density connection.

The connection method introduced by Casio Computer, CO., LTD. is the one connecting conductive particles each covered by an insulating coating using an ACP (anisotropic conductive paste) mixed therewith. Compared with the conventional ACF, the resulting connection density will be expectantly high.

Even if these new connection methods are applied, it is still difficult to suppress the cumulative error associated with the processing processes and the surrounding environment as long as organic films such as polyimide or polyester films are used. In order to respond to connection of the future with pitch of 100 μm or lower, there needs comprehensive development including materials and processing methods.

CHECKUP

Checkup of drive LSI after bonding in the TAB packaging is becoming a problem as the packaging density of the drive LSI becomes higher.

At the time of checkup of the drive LSI, if the between-electrode pitch becomes 100 μm or lower, it becomes difficult to make a contact using a conventionally-popular prope

card including tungsten carbide needles arranged in line. Thus, a development possibility is such a measurement technique that not every terminal but only main terminals are contacted to prevent faulty mixture.

Checkup after bonding is done using a checkup pad provided around the drive LSI packaging section of a tape carrier as shown in FIG. 5. This checkup pad is torn off after the checkup is through. As the drive LSI includes the more electrodes, problems are beginning to come to the surface, i.e., increase of the area occupied by the checkup pad, and the contact unstability at the time of checkup.

Development of checkup means achieving stable contact with many electrodes located in a small area without including a checkup pad leads to improvement of the measurement speed and substrate usage efficiency, considerably contributing to price reduction of TAB packaging. As one possible means, there is checkup means so far developed by Japan Synthetic Rubber Co., Ltd. using a rubber connector of high resolving power.

EQUIPMENT DEVELOPMENT FOR COG

With the COG packaging method, a drive LSI is directly packaged onto a glass substrate of a liquid crystal panel. This is considered promising as packaging means with respect to the drive LSI of the high-definition-pixel liquid crystal panel.

Since drive LSI packaging (connector scheme) of liquid

crystal televisions was put on the market by Citizen Watch, CO., LTD. in 1983, various COG packaging methods have been developed as shown in FIG. 6.

Among these packaging methods, as the COG packaging method having been actually used up to now, there are two schemes excepting the connector scheme: one is a wire bonding scheme; and the other a scheme using a conductive paste. FIG. 7 shows an exemplary COG packaging method.

COG VARYING IN TYPE

A brief description is made about the respective COG packaging methods shown in FIG. 6.

1. Wire Bonding Scheme

On a glass substrate of a liquid crystal panel, a wire-bondable metal pattern is formed (e.g., Al, Au) so as to connect a drive LSI thereto by wire bonding.

2. Flip Chip Scheme

On a glass substrate of a liquid crystal panel, a solder-connectable metal pattern is formed so as to directly facedown-bond a drive LSI formed with a solder bump.

3. LMC (low melting point metal connection) Scheme

Directly to an electrode pattern on a glass substrate of a liquid crystal panel, a drive LSI having an AU bump formed with an In alloy is facedown bonded.

4. Connector Scheme

Using a rubber connector, a pattern on a glass substrate of a liquid crystal panel and a drive LSI are connected together by pressure welding.

5. Conductive Paste Scheme

Using a conductive paste, a pattern on a glass substrate of a liquid crystal panel and a drive LSI formed with an Au bump are connected together.

6. SBB (stud bump bonding) Scheme

Using a conductive paste, a pattern on a glass substrate of a liquid crystal panel and a drive LSI including an Al electrode formed with an Au ball are connected together by wire bonding.

7. ACF Scheme

Using an ACF or ACP, a pattern on a glass substrate of a liquid crystal panel and a drive LSI formed with an Au bump are connected together.

8. MBB (microbump bonding) Scheme

A pattern on a glass substrate of a liquid crystal panel and a drive LSI formed with an Au bump are connected together by pressure welding utilizing shrinkage stress of an UV curing resin disposed in a gap formed between the liquid crystal panel and the drive LSI.

9. Conductive Particle Scheme

Onto an electrode pattern on a glass substrate of a liquid crystal panel, a paste including conductive particles derived by applying an Au plating to organic beads is print-coated for

connection with a drive LSI. Alternatively, to a pattern on a glass substrate of a liquid crystal panel, a drive LSI in which an electrode section is previously attached with conductive particles derived by applying an Au plating to organic beads is connected by pressure welding using an optic curing resin.

As such, although there are various types of schemes, for practical use of the COG packaging, due consideration must be given to the process design in consideration of heat resistance of the liquid crystal panel itself, mechanical strength of the glass substrate, and the patterning processing (materials and wiring density) and structure causing no price increase of the liquid crystal panels.

INTEREST LOSS

Here, as to the COG packaging, its characteristics and challenges are studied, starting with its advantages.

1. Advantageous for price reduction of packaging - compared with TAB packaging, for example, price reduction is possible for liquid crystal panel modules thanks to the fewer number of components, and the fewer number of processes. Such effects become apparent because the liquid crystal panel of a higher pixel level has the more drive LSI.

2. Advantageous for drive LSI packaging of high-definition panel - a pattern for drive LSI packaging can

be formed simultaneously with a pixel electrode pattern format for the liquid crystal panel. Accordingly, it allows forming the pattern pitch 50 μm or lower, and at the time of packaging of a drive LSI of the fine-pitch liquid crystal panel of a higher pixel level, there is no need to increase the size of the liquid crystal panel.

3. Advantageous for size and width reduction of liquid crystal panel module - a drive LSI is directly connected onto a glass substrate of a liquid crystal panel. This thus increases slightly the size of the liquid crystal panel (with the method of TAB, for example, required for connection is 2 to 3 mm, but with COG, required for connection is about 6 to 10 mm), but as the liquid crystal panel module itself, size reduction is possible in terms of area and capacity.

4. Advantageous for yield and quality stability with the fewer connection points - because a drive LSI is directly connected to a glass substrate of a liquid crystal panel, the liquid crystal panel module can be formed with the least connection points, being advantageous for improving the packaging yield and quality stability.

CHALLENGES OF QUALITY, EQUIPMENT, AND CHECKUP

On the other hand, there are some challenges left as below.

1. The connection pattern of a drive LSI of a liquid crystal panel gets complicated, and the resistance value of

the pattern wiring varies a lot, affecting the display quality of the liquid crystal panel.

2. The COG is the newly developed packaging method, and varying in manner. Accordingly, it is difficult to deal with the existing packaging equipment, and there needs to develop any new packaging unit to put the COG packaging method in practical use.

3. Checkup of fine-pitch multi-terminal drive LSI and liquid crystal panel has a difficulty with the conventional method using tungsten carbide needles, and thus there needs to develop any new measurement means.

4. Many of the COG packaging methods establish connection between an ITO pattern and a drive LSI using organic materials by bonding or compression bonding. Thus, compared with the conventional time-proven connection method utilizing between-metal diffusion, resulting in anxiety for quality.

PROBLEMS OF POSITIONING AND ORGANIC MATERIALS CAN BE HANDLED

As to the packaging equipment, for the purpose of plurally chip-packaging a fine-pitch multi-terminal drive LSI, various many development dimensions are included. Among all, the most difficult problem of positioning accuracy can be solved by utilizing clarity of the glass substrate. The possibility of mass production unit can be handled rather easily.

As to the quality problem of COG packaging, even if organic

materials are used for bonding or compression bonding, appropriate material selection and appropriate structure design will derive the packaging reliability exceeding at least the reliability level of the liquid crystal panels. This is understandable by the time-proven accomplishments that various types of organic materials have been already used for connection in liquid crystal panel modules, i.e., the conductive adhesive actually used for drive circuit connection and Ag point connection of liquid crystal panels has so far caused no problem, and with the currently-popular TAB packaging method, a liquid crystal panel and a dive LSI have been connected together using a thermoplastic or thermosetting ACF.

If the reliability level of the liquid crystal panel module is at least satisfying the following requirements, there may not cause any problem in practical use.

- Storage under high temperature and high humidity

60°C, 90% RH1000 hours

- Storage under high temperature

85°C 1000 hours

- Storage under low temperature

-30°C 1000 hours

- Temperature Cycle

-30°C/80°C, 500 times

WANT NEW MEASUREMENT METHOD

Checkup of a drive LSI chip and checkup of a liquid crystal panel in the COG packaging will be the significant challenge of the future. As the drive LSI gets lower in between-electrode pitch and includes more terminals, using the conventional probe card poses limitations for measurement of the drive LSI.

At the time of measurement of liquid crystal panels, the measurement pattern sections are concentrated similarly to the drive LSI electrode. As a result, similar to the drive LSI, this poses contact limitations using the probe card. Thus, it is impossible to deal therewith without developing any new measurement means to take the place of the conventional measurement means.

As such, desired are any new measurement means achieving high faulty detection ratio with the fewer contact points, and any new method possibly deriving stable contact with multi-terminal electrodes.

COG ACHIEVES HIGH AREA EFFICIENCY

The smaller panels are more influenced on the number of liquid crystal panels by the increase of panel area due to COG packaging. For the larger panels, on the other hand, such an influence is hardly observed.

COG achieving the reduction of LSI chip size contributes to downsizing of the liquid crystal panel modules, and also

affects the drive LSI in number from a wafer. As a result, it considerably contributes to price reduction of the drive LSI.

The drive LSI chip for COG packaging can be applied with a pixel electrode pattern processing in a fine manner for connection. Thus, it allows not only pitch reduction between the electrodes but also zigzag arrangement and matrix arrangement. As such, various methods can be adoptable for reducing the chip area of the drive LSI.

A comparison is now made between a chip area of a currently-available drive LSI for COG and that of a drive LSI for TAB based on an area occupied per one output. The comparison result shows that the drive LSI for TAB is 0.21 to 0.4 (mm^2/output), and the drive LSI for COG is 0.18 to 0.25 (mm^2/output). As such, the area efficiency of the drive LSI for COG is considerably high.

As is described in the foregoing, the COG packaging is suitable for packaging a drive LSI in a liquid crystal panel.

Before such COG packaging is going into full-scale production, requirements has to be satisfied first, i.e., widespread applications of a high-definition liquid crystal panel with pixel electrode pitch being 100 μm or lower, matching between the packaging structure and materials to be used, assured reliability of quality, and the like.

COG WILL BE ESSENTIAL

As to drive LSI packaging of liquid crystal panels of the future, although not the same in level, both TAB packaging and COG packaging have to address many challenges such as a technology of high-density multi-terminal connection, an inspection technology of LSI and liquid crystal panels, reliability technology, and the like.

With packaging for color liquid crystal panels mainly for OA and super-high-definition liquid crystal panels such as view finders, the high-density connectability of the COG packaging standing out from others will be essential. In the near future, this COG packaging technology will be adopted to a wide range of applications, starting with the high-definition panels.

The COG packaging technology is the one started from the drive LSI packaging of the liquid crystal panels. This technology is recently considered promising in fields in which the conventional connection technologies (wire bonding, flip chip bonding, TAB) have seen the difficulty in connection, i.e., an application requiring high-density multi-terminal connection such as printer heads and image sensors, an application of multi-chip modules plurally packaging a multi-chip LSI, and the like.

With respect to such fields varying in type, there needs to keep higher the packaging quality level, and develop any

packaging means having better efficiency, for example.

REFERENCE LIST

1. INOUE, "Packaging of multi-pin LSI, many have been commercially practical", Nikkei Micro Device, July, 1989 : no. 49, pp. 49-52

2. INOUE, "packaging Technology in Liquid Crystal Panel (COG)", "Full-Color Liquid Crystal Display Technology", Torikeppusu (phonetically written), February, 1990.

FIG. 1

Application-basis relationship between screen size and pixel electrode pitch of liquid crystal panel

FIG. 2

Drive LSI packaging technology of liquid crystal panel

(a) connector connection between packaged or resin-sealed LSI and electrodes on glass substrate

(b) TAB (tape automated bonding) technology

FIG. 3

Side-basis relationship between pixel electrode pitch and the number of pixel electrodes

Also shown is the number of terminals connectable at one time

FIG. 4

Process concept of TAB packaging

FIG. 5

Checkup pad after bonding

Provided around drive LSI packaging section of tape carrier

FIG. 6

Comparison of COG packagings

ガラス基板 glass substrate

スプリング	spring
フレーム	frame
ラバー・コネクタ	rubber connector
ワイヤボンディング	wire bonding
コネクタ	connector
フリップチップ	flip chip
金属	metal
Ａuバンプ	Au bump
ガラス	glass
Ｉn合金	In alloy
ＳｂＳnバンプ	SbSn bump

表（Ｐ１８６）

接続手段	connection means
駆動ＬＳＩ	drive LSI
液晶パネル	liquid crystal panel
ボンディング	bonding
リペア性	repairability
利点	advantage
欠点	disadvantage
電極状態	electrode condition
電極ピッチ	electrode pitch
パターン状態	pattern condition
温度	temperature
加圧力	pressure force

他 others

Ａｕワイヤ Au wire

Ａｌパッド Al pad

最小１５０μm minimum 150 μm

実装設備が既存設備で対応可 any existing equipment is usable for packaging equipment

バンプ形式不要 no need for bump form

パターンメタライズが不可欠 pattern metalization essential

ゴム・コネクタ rubber connector

Ａｕバンプ Au bump

ＩＴＯ（透明電極） ITO (Indium-tin oxide)

室温 room temperature

パッド pad

低温・低圧力の実装が可能 possible packaging under low temperature and low pressure

部材数が多い many components

半田 solder

Ｐｂ/Ｓｎバンプ Pb/Sn bump

パターン・メタライズが不可欠 pattern metalization essential

高温接続となる result in high temperature connection

Ｉｎ合金 In alloy

Ａｕ/Ｉｎバンプ Au/In bump

Ｉｎの安定形成 In stable formation

表（Ｐ１８７）

ガラス基板	glass substrate
封止樹脂	sealing resin
Ｃｕバンプ	Cu bump
ガラス	glass
ペースト	paste
Ａｕボール	Au ball
ＵＶ硬化樹脂	UV curing resin
Ａｕバンプ	Au bump
導電粒子	conductive particle
導電ペースト	conductive paste
Ｃｕ/Ａｕバンプ	Cu/Au bump
パッド	pad
ペーストの広がりコントロールが難しい	difficulty in paste spread control
Ａｕバンプ	Au bump
良品ＩＣのみにバンプ形成可	bump formation allowed only to conforming IC
１電極ごとにバンプ形成	bump formation on electrode basis
高い接続分解能を得ることが難しい	difficulty in deriving high connection resolving power
室温	room temperature
ＵＶ光	UV light
部材数が最も少ない方式	method requiring the fewest components
導電粒子	conductive particle
Ａｌパッド	Al pad
バンプ不要	no bump required

Ａｌと安定接続が難しい difficulty in stable connection with Al

Ａｕパターン Au pattern

FIG. 7

Exemplary COG packaging